Consideration Of Mechanical Chip Crack On FBGA Packages

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Abstract

The laminate type FBGA package is one of the advanced solution of economic chip scale package, and has started to be used for applications that require low profiles and small areas, such as cellular phones or hand held products. IBM started to use "Mold & Saw" or "Matrix" type FBGA package, a technology to align plural numbers of semiconductor chips on a segment area of the laminate, wire bond, transfer mold, then finally singulate by a dicing saw. The ability to dice the package size independent to the molding chase or punching equipment is the largest benefit of this technology.

During the development stage, IBM had observed a phenomenon that the chips were completely separated into two or more segments. Initially the root cause was suspected to be the CTE difference of the materials that generates mechanical warpage to the laminate, but simulational analysis showed no impact.

To solve the phenomenon, we discovered the correlation of the laminate profile, solder mask thickness variations, and mechanical stresses on the chip surface. A "bath tub" shaped solder mask profile at the center of chip placement area on the laminate may cause excessive pressure on the chip during transferring mold compound, and result in chip fractures. Experiments using several variations of laminate profiles were used, and confirmed the larger profile can generate chip cracks. This paper contains details of the phenomenon, solution and effectiveness.

Introduction

The demand in the market is continuously strong for a small, thin, lightweight, high density, high quality and low cost semiconductor package, especially in telecommunication and handheld products. To address this need, IBM started to use the FBGA (Fine Pitch plastic BGA) package, a low profile, high ball count and semi-chip scale solution.

The FBGA charactersitics that IBM developed are as below.

1. Ball pitch 0.8 mm or 0.5mm
2. Package size 13x13mm or 15x15mm
3. Package height 1.4mm maximum
4. Ball count 176, 208 or more
5. Mold and Saw process

The construction is similar to an industry standard PBGA (Plastic Ball Grid Array) package. On a BT resin base substrate strip coated by solder mask material, a semiconductor chip is attached , wire bonded, and transfer molded. In addition, common manufacturing processes and equipments can be utilized.

The technical challenges for FBGA package are ;

1. Use of a 0.26mm thick substrate to obtain thin package height
2. Application of mold & saw process type singulation to obtain low cost productivity
3. Design of a 15 x 15mm body for high signal pin count
4. Managing JEDEC MSL (Moisture Sensitivity Level) 2A with reflow temperature of 240 deg C
5. Targeting 260 deg C reflow temperature for the coming Pb-free programs in 2001.

FBGA Manufacturing Process

A standard PBGA molding process is to set a molding cavity per each unit on the substrate strip. Therefore, the strip requires areas around the unit to allow for the punching or routing singulation process. This means each package design requires different molding equipment for each package outline size, which increases the manufacturing cost.

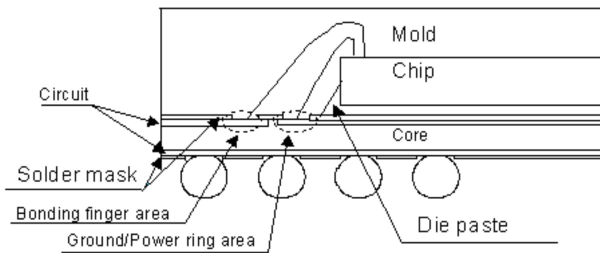
Instead of, FBGA applys a mold & saw singulation method, a technology to align plural numbers of semiconductor chips on a segment area of the substrate, wire bond, transfer mold a large section of the strip, then finally singulate by a dicing saw. The largest benefit of this technology is the ability to dice the package size independent to the molding chase or punching equipment. For comparison, a 15x15mm PBGA currently allows for 10 units per substrate strip, while an FBGA strip allows for between 30 to 60 units depending upon the strip width.

Therefore, the largest challenge from manufacturing point of view is how to manage the wide substrate strip. Detail concerns are as below.

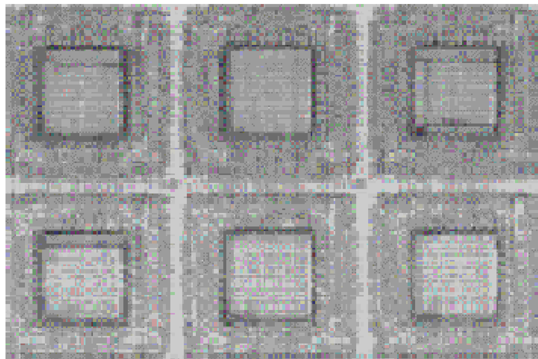
1. Strip warpage caused by mold material shrinkage, which affects ball coplanarity
2. Wire sweep during transfer molding caused by high transfer pressure
3. Circuit shorting caused by insufficient singluation accuracy or strip warpage.

Chip Damage

During the development stage, an abnormal phenomenum was discovered. Semiconductor chips inside the mold compound were completely desroyed by one or more cracks after assembly as shown in Figure 1. This phenomenum was observed by SAT (Sonic Acoustic Tracing). No external mold cracks, separations, warpages or coplanarity defects were detected on these modules containing cracked chips. And all cracks were located near to the chip edges, not at centers. Each assembly process was analized and monitored. From this, it was confirmed the chip cracking occures within the molding process.



(a) Construction of FBGA



(b) SAT image of strip

(c) Cross section photo

Figure 1. Chip Crack

First, the material CTE difference was suspected to be the root cause. It is well reported that chip cracks can be caused by a tensile stress on the silicon, and the maximum stress constrain point in the package is the chip center and chip corner. This is explaned in the following equaltion.

$\rightarrow = E\ T\ (a_2 – a_1)$

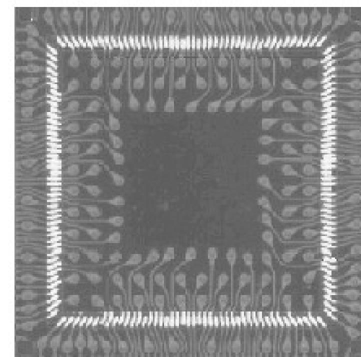
$\rightarrow$: stress at chip center (assuming large substrate strength)

E : young ratio

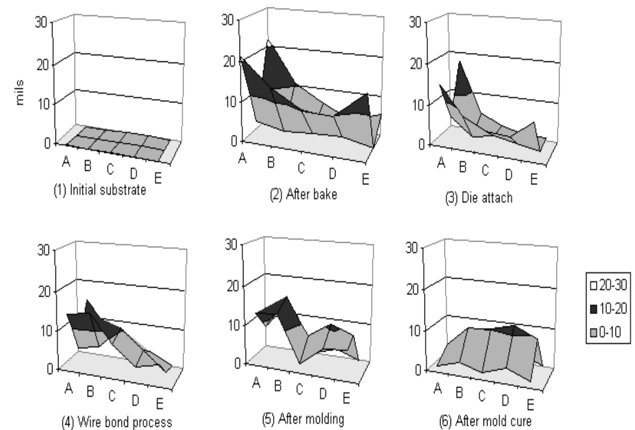
T : temperature delta

a_2 , a_1 : CTE of substrate, chip

Considering the CTE of silicon is 3 - 4 ppm and of a standard mold compound is 7 – 15 ppm, there is a delta of approximately 3 – 12 ppm. The effect of this CTE delta can be shown in substrate strips after a mold cure process, which has a temperature delta of approximately 150 deg C between the heated condition and ambient room temperuatre. However, the location of failure, as shown in the SAT image in Figure 1, is not located at the center.



(a) Image of substrate design



(b) Substrate strip profile

Figure 2 . Substrate Strip Profile

Next, the correlation between substrate strip warpage and the mechanical stresses during molding process was analyzed. Figure 2 shows the substrate strip warpage difference, measured from incoming condition until the mold curing process. A straight substrate strip was deformed into a “U” shape by the high temparature during chip placement and wire bond processes, then warped into a “frowning” profile by the mold material shrinkage after mold curing process. However,

it is difficult to state the evidence of correation between the strip warpage and the point at which chip cracks were seen. The maximum tensile stress should be at the chip surface to generate cracks from the top. But as shown in the cross section photo in Figure 1, all of the cracks propagate from the bottom side of the die.

Additionally, several types of mold compound covering various CTE values were applied. But no change in the crack shape, location, or defect ratio was detected.

Substrate strip profile

As the second step, the substrate strip construction was the focus of analysis. The substrate design laminates copper circuits on both sides of a BT resin core, which is then covered by solder mask material. Also, the molding die tool is heated to between 150 to 180 deg C to transfer the melted mold compound into the cavity area. When the mold compound reaches to the end of the cavity, the pressure on the substrate or die is maximum in the z-axis.

Meanwhile, manufactures ought to apply back etch on the copper layer and then apply the solder mask as thin as possible, to contribute to the thin package requirements. But this generates varaeties of solder mask profiles on the laminate.

Moreover, a bath tub shape solder mask profile could be observed within the chip placement region on a raw substare strip. It was confirmed that the thick solder mask area has copper circuits underneight, and that the thin aera has no copper patterns. Figure 3 shows an example of the solder mask thickness of 59um under the chip corner, but 38um at the center. If there is pressure on the top of the chip, it is possible to bend the chip to the shape of the bath tub profile.

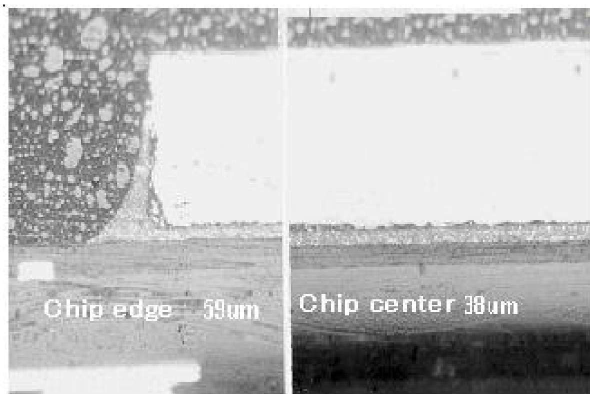


Figure 3 Cross section view at chip center and edge

Modeling

Why cracks occur near chip edges not at the center, and what is the correlation with solder mask profile are discussed. The circumstances within the molding tool can be explained as shown in Figure 4. The solder mask with bath tub shape depth of y_{max} exists on both surfaces of the substrate. The die attach material will be soften under the condition of 150 to 180 deg C, because of its Tg lower than 100 deg C. This condition allows the silicon chip to be bent by the mold transfer pressure.

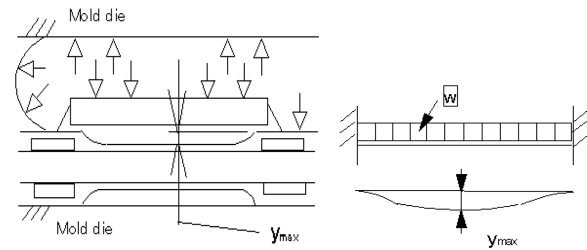


Figure 4 . Chip Crack Mechanism

First, Finite Element Analysis was performed to understand the Von-Mises and x-axis stress distributions on chip bottom surface, placed on a bath tub shaped solder mask. Figure 5 shows a quarter model. Maximum compression stress is located at the interface of the solder mask profile changes, where the copper pattern ends. The chip center also shows a compression stress, which is correlated to the maximum depth of solder mask profile.

A tensile stress area is detected. It is located between the chip center and the interface of thin solder mask. In the case of silicon material, tensile stress is the main factor to observe line cracks.

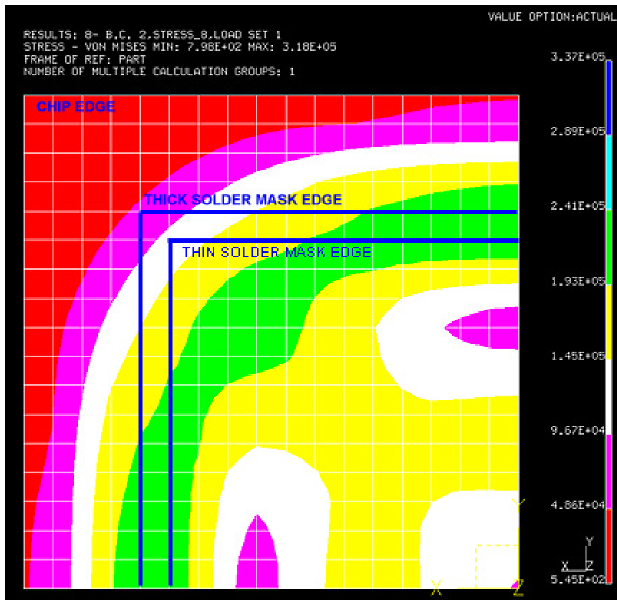
Secondly, the correlation of solder mask profile and mold transfer pressure is discussed. The strength of materials equation can be applied to the chip crack mechanism by treating the die as a simpified, constrained beam. The mold transfer pressure can be treated as an uniformly distributed load across the beam. Hence, a simplified case of statically indeterminate beam with an uniformly distributed load can be applied. The equation of laminate profile y_{max} is described as below.

$$y_{max} = w L^4 / (384 E I)$$

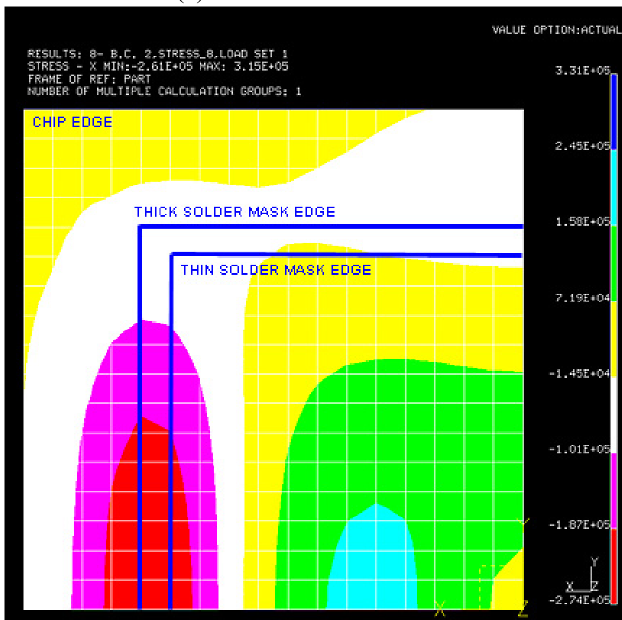
$$y_{max} = 0.11798 \times 10^{-10} w L^3 \text{ (mm)} \qquad \text{(i)}$$

w : pressure on the chip surface
L : chip length (mm)
E : Modules of elasticity
I : Moment of inertia

Under assumption of 2 MPa silicon chip fracture strength, the chip deflection y should be less than y_{max} to avoid chip cracks. For example in case of 7.4mm sized chip, a 10um deflection is the threshold to observe the occurance of chip crack.



(a) Von-Mises destribution



(b) X-axis stress destribution

Figure 5 . Simulation result

Experiment

To validate the modeling, substrates with varieties of solder mask profiles were collected, and their performance was monitored using SAT.

The results were plotted as shown in Figure 6. Substrates containing a deep solder mask profile showed chip cracks (marked as "X" in Figure 6), while substrates containing a shallow solder mask profile showed no cracks (marked as "O" in Figure 6). For comparison, equation (i) applying silicon fracture strength 2MPa is plotted in the graph. In the case of solder mask profile depth is larger than the fracture line, the chip could be destructed.

Moreover, the locations of cracks on the chip were confirmed to be similar area of the results of the simulation. And the correlation of the profile depth and occurance percentage was observed. For example regarding the 7.4mm chip assembly case, the profile depth and defect ratio was confirmed as 50% for depth of 20um, 17% for 14um, and 0% for 3um. Approximately 300 samples per cell were monitored.

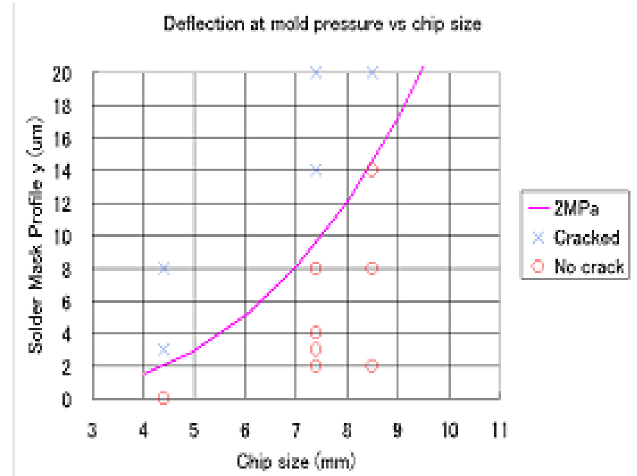


Figure 6 . Experiment

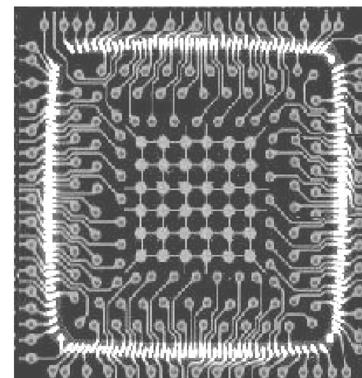


Figure 7 . Solutions

Observation

The FEM simulation result shows an area of tensile stress exsiting under the silicon chip, between the chip center and the edge of the solder mask profile changing line. The area of tensile strength occures in the same location in which chip cracks were observed. This means the unstable solder mask profile may generate bending stress during mold transfer process.

The only solution to prevent chip crack damages is to have a more stable solder mask profile. The considerable candidate methods are (1) to apply a rich amount of solder mask and stabilize the thickness, (2) to place a dummy copper layer underneight the concerned area to prevent varieties of solder mask thickness as shown in Figure 7.

The results were applied in production. As a short term solution, substrates that have a maximum solder mask profile depth of 3um were used. And as a permanent solution, new substrates with dummy copper patterns were applied on both surfaces. These solutions showed improvements in defect ratio from approximately 20% during qualification stage into 0 % during production stage.

Conclusion

We have presented an unique phenomenon detected during FBGA development stage, how we analized the correlation of mechanical stresses, and the validation work to solve. This is one of the activities which contributes to mass-production quality and reliability.

Effectiveness

The results can be considered as a factor for future products which have processes of transfer molding pressure during assembly. In case of a FBGA package with multiple stacked chips inside, bottom-chip destruction can be observed as shown in Figure 8. The breaking point of the bottom chip is near to the top-chip edges. Unblanced mold compound pressure from horizontal axis is assumed to be one of the factors.

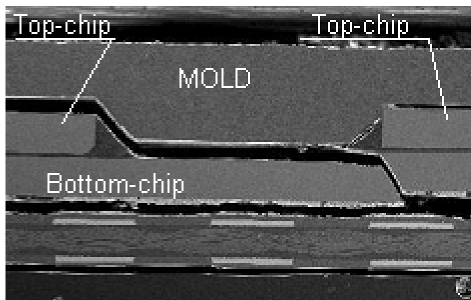


Figure 8 . Concerns to chip stack products

Acknowledgments

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